FINFET
FOR SUB-22NM TECHNOLOGY NODES

S. Biesemans
VP Process Technology & Strategy

imec

Imec Introduction

Founded: 1984

CAMPUS

Revenue 2011: 300Meuro

Total: 8000 m^2 Clean Room

ADV. SCALING PROGRAM PARTNERS

Memory IDM

SAMSUNG

Micron

hynix Semiconductor

ELPIDA

PSC

Logic IDM

intel

Panasonic

Foundries

tsmc

SAMSUNG

GLOBALFOUNDRIES

Fablite

SONY

FUJITSU

NXP founded by Philips

Fabless

QUALCOMM

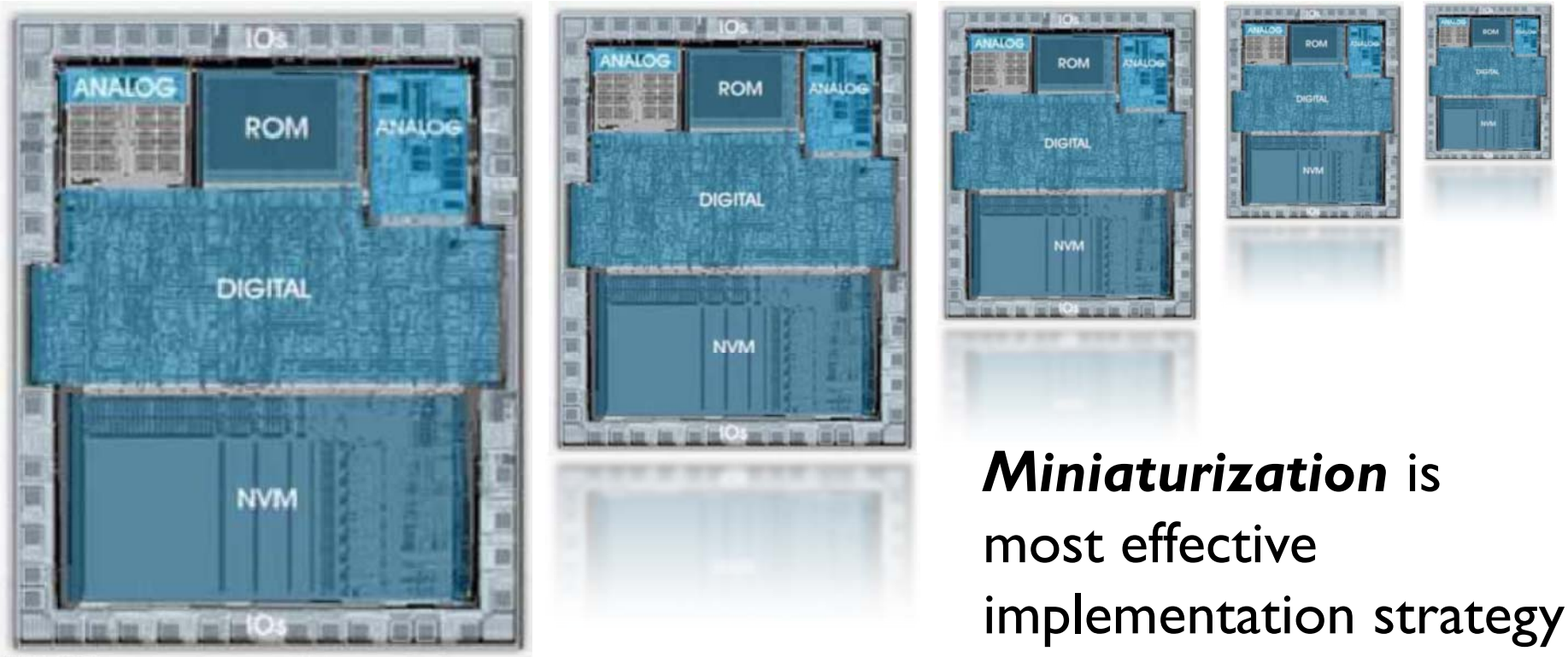
XILINX

NVIDIA

ALTERA

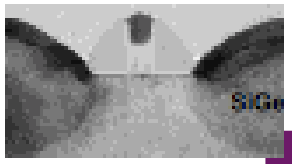
Continuing Moore's law

Moore's law (1)=	Double the number of devices every 2 years



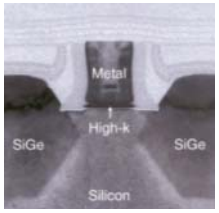
Miniaturization is most effective implementation strategy

LIKELY LOGIC ROADMAP



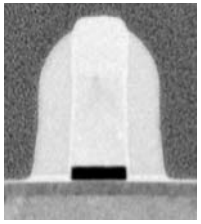
65 nm

planar
SiON
stressor



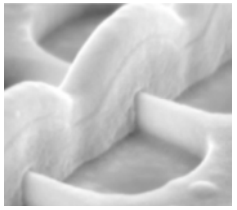
45-40 nm

planar
Poly-SiON
RMG



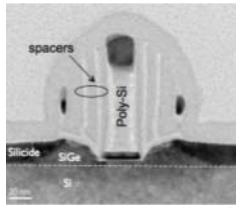
32-28 nm

planar
Poly SiON
RMG
MIPS



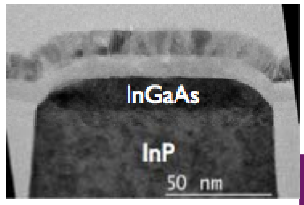
22-20 nm

Planar, FiNFET
RMG



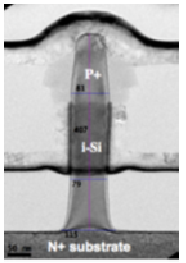
16-14 nm

FinFET, UTBSOI
RMG
SiGe



11-10 nm

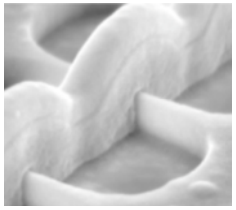
FinFET,
Nanowire
SiGe, Ge, IIIV

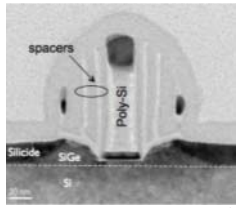


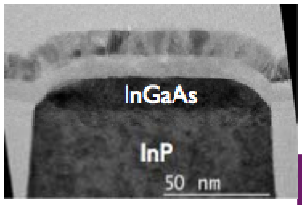
<10 nm

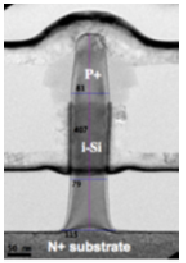
Nanowire,
TFET
Ge, IIIV, ...

LIKELY LOGIC ROADMAP









16-14 nm

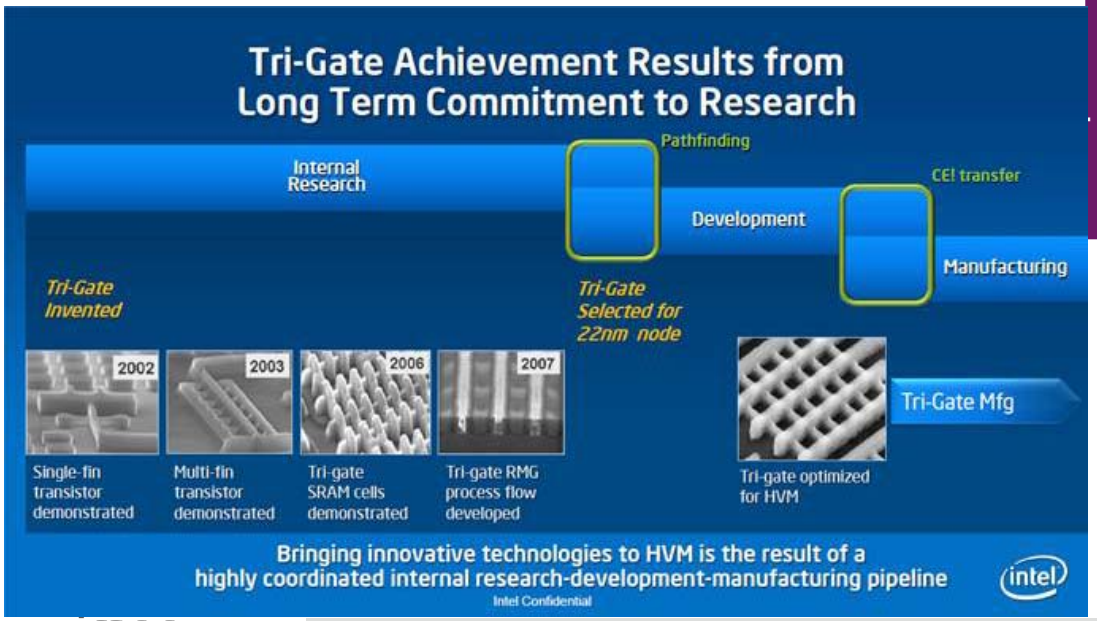
FinFET-UTBSOI
RMG
SiGe

11-10 nm

FinFET,
Nanowire
SiGe, Ge, IIIV

<10 nm

Nanowire,
TFET
Ge, IIIV, ...

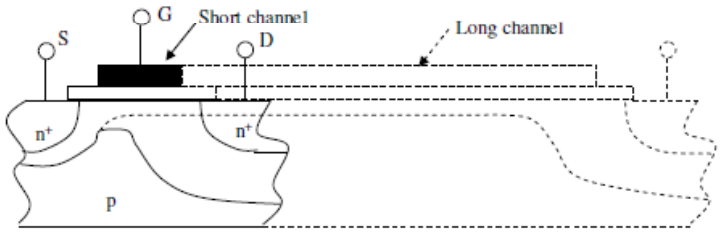


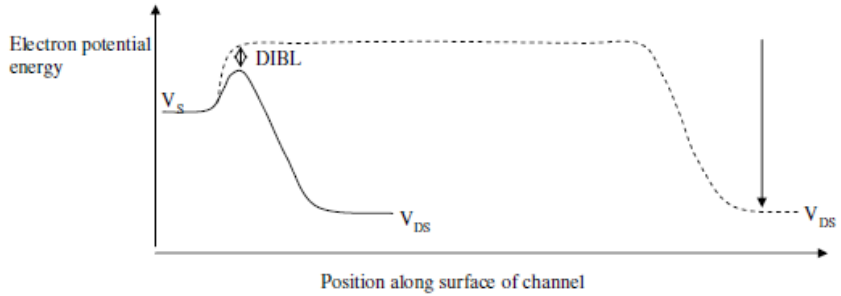
Why FinFET ?

DEVICE POWER
HOW TO TACKLE THE PROBLEM?

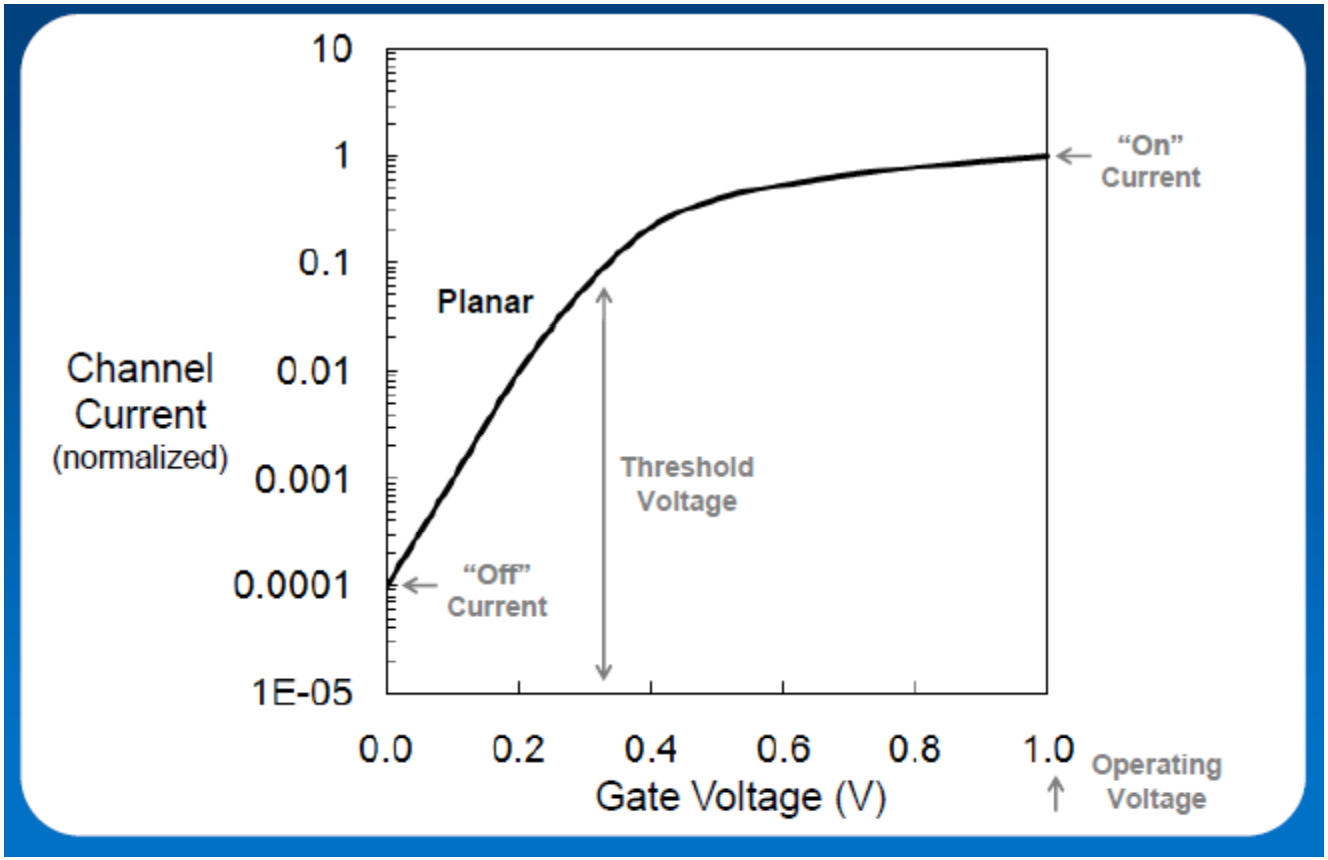
Sub-V_T Leakage

<u>Solution</u> → New Architecture
Fully Depleted Devices
for better
Short-Channel control



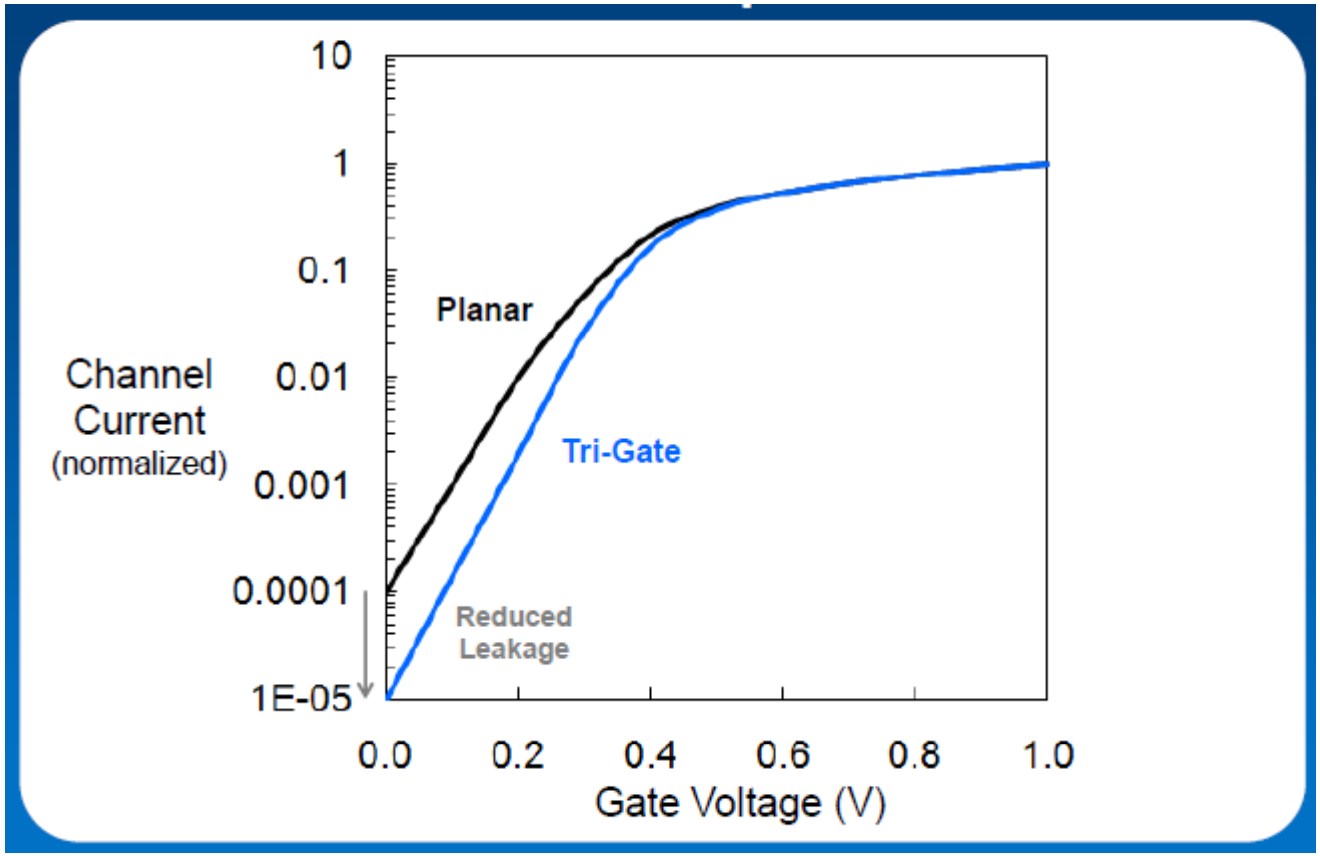


TRANSISTOR



Source: Intel May'11

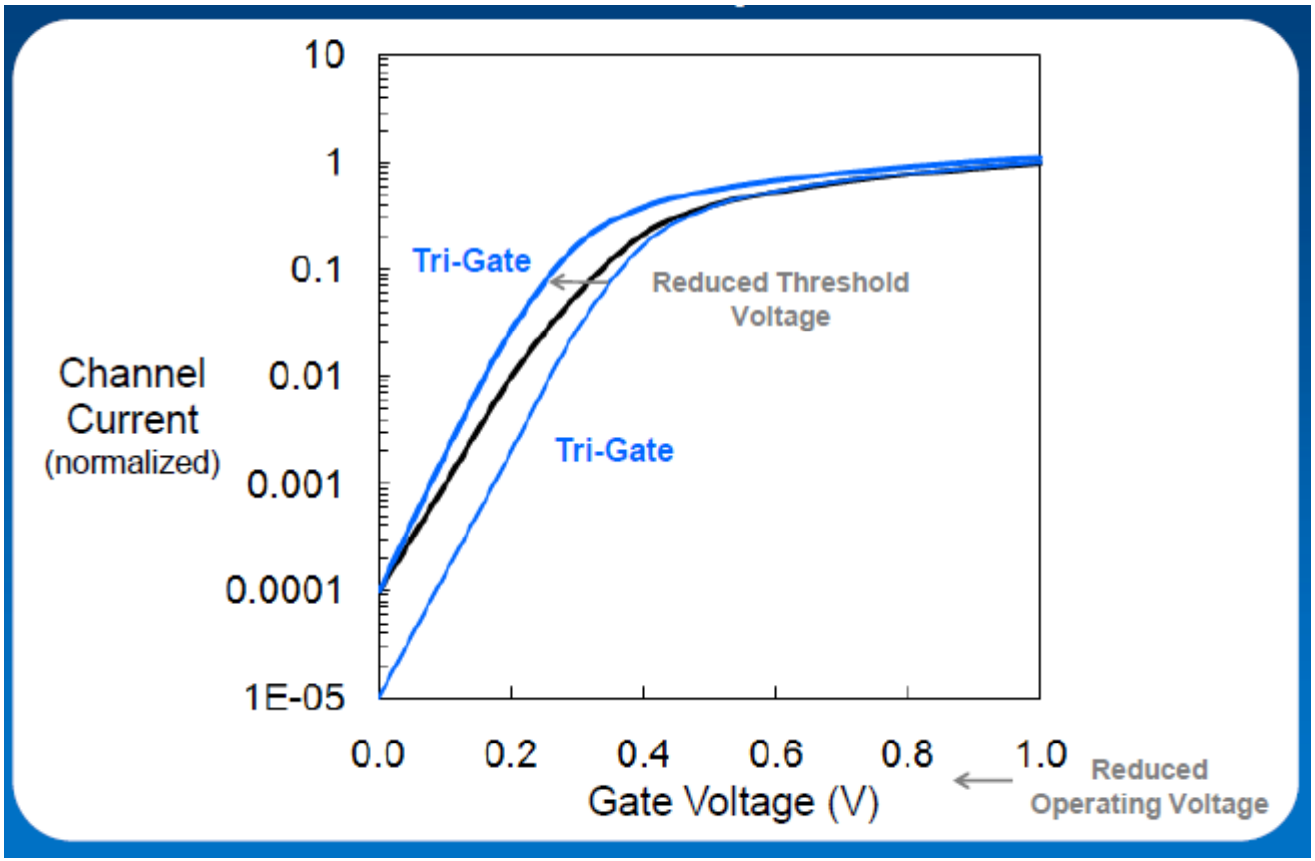
TRANSISTOR



Source: Intel May'11

Fully depleted channel -> Steeper slope -> ***Reduced leakage current***

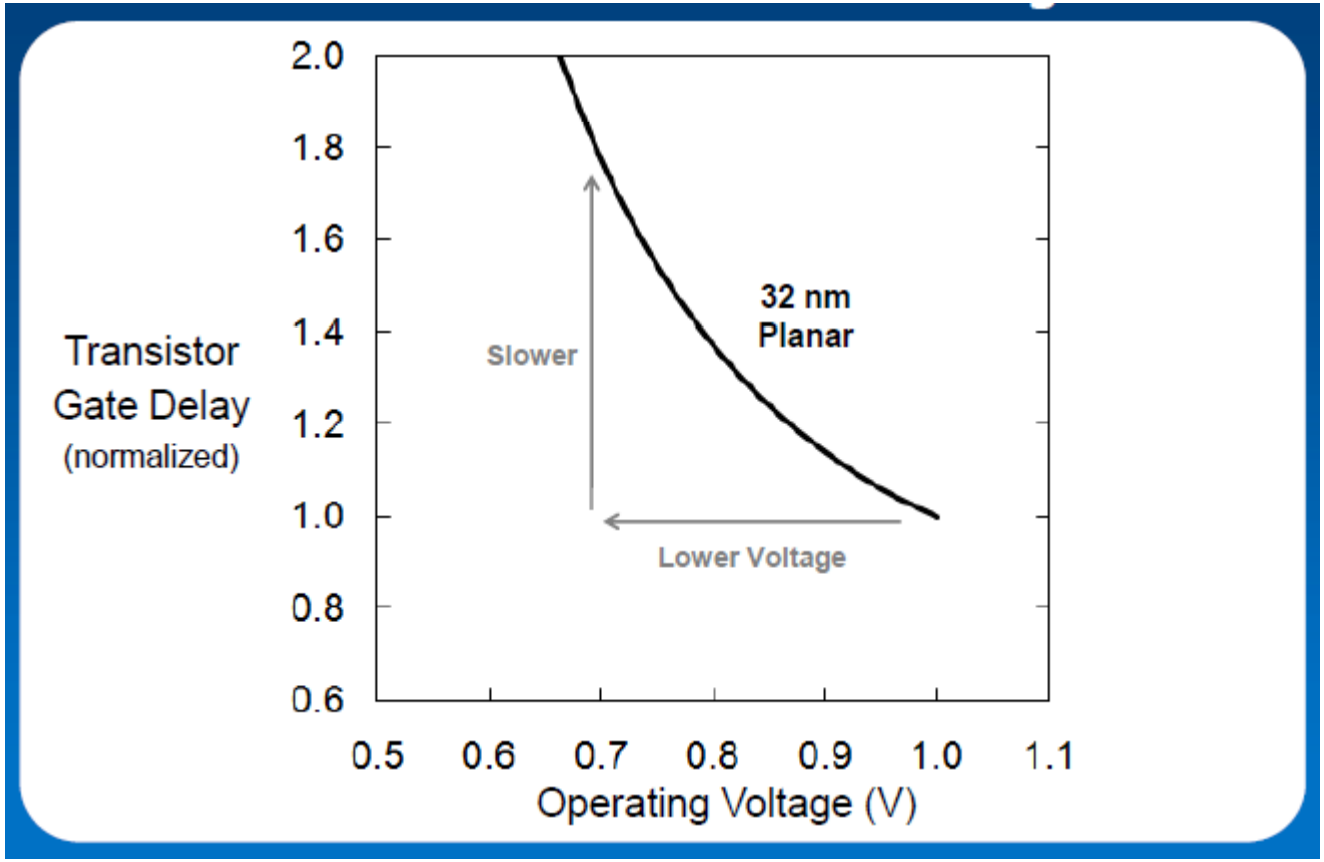
TRANSISTOR



Source: Intel May'11

Fully depleted channel -> Steeper slope -> *Target **lower threshold voltage**, improve circuit speed*

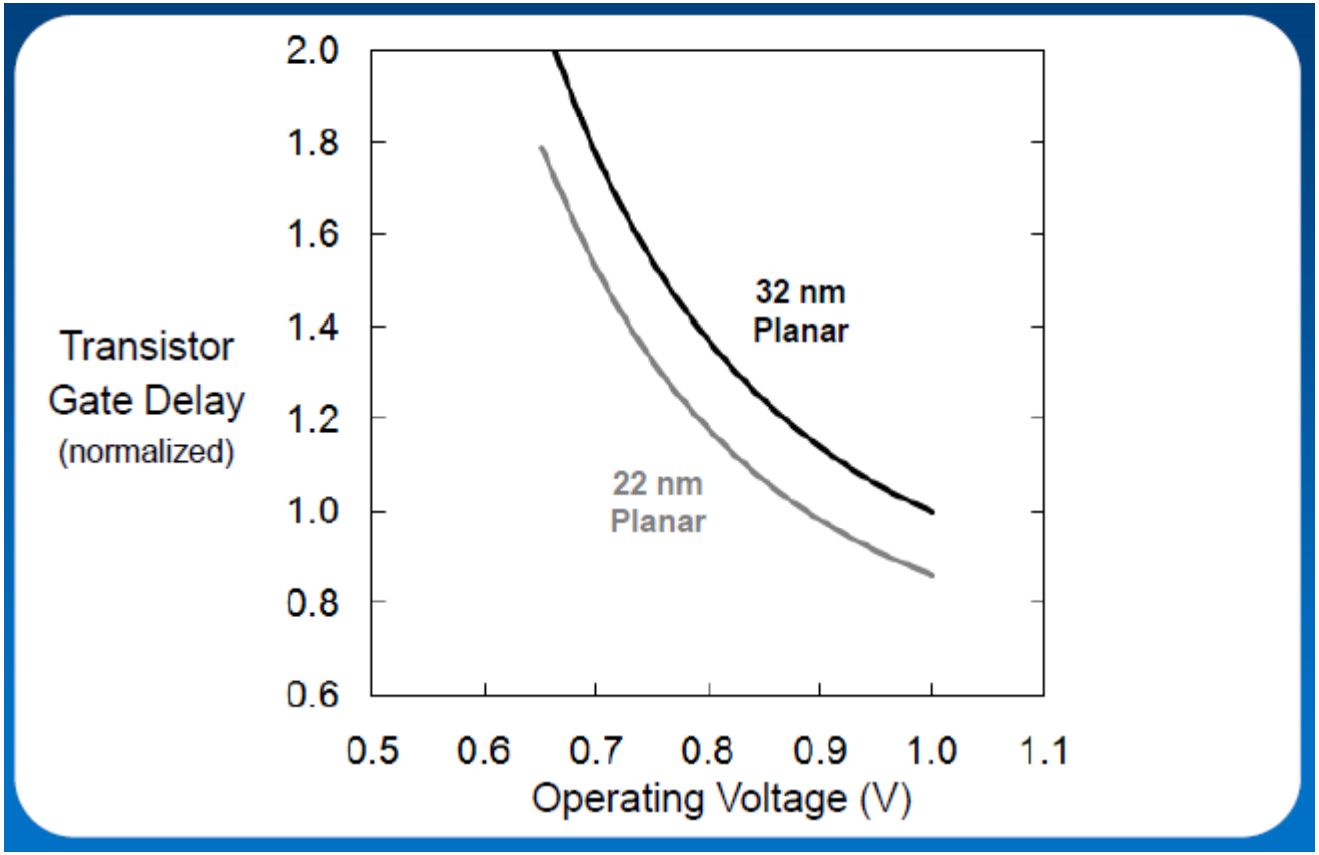
GATE DELAY



Source: Intel May'11

Circuits slow down as Vdd reduces

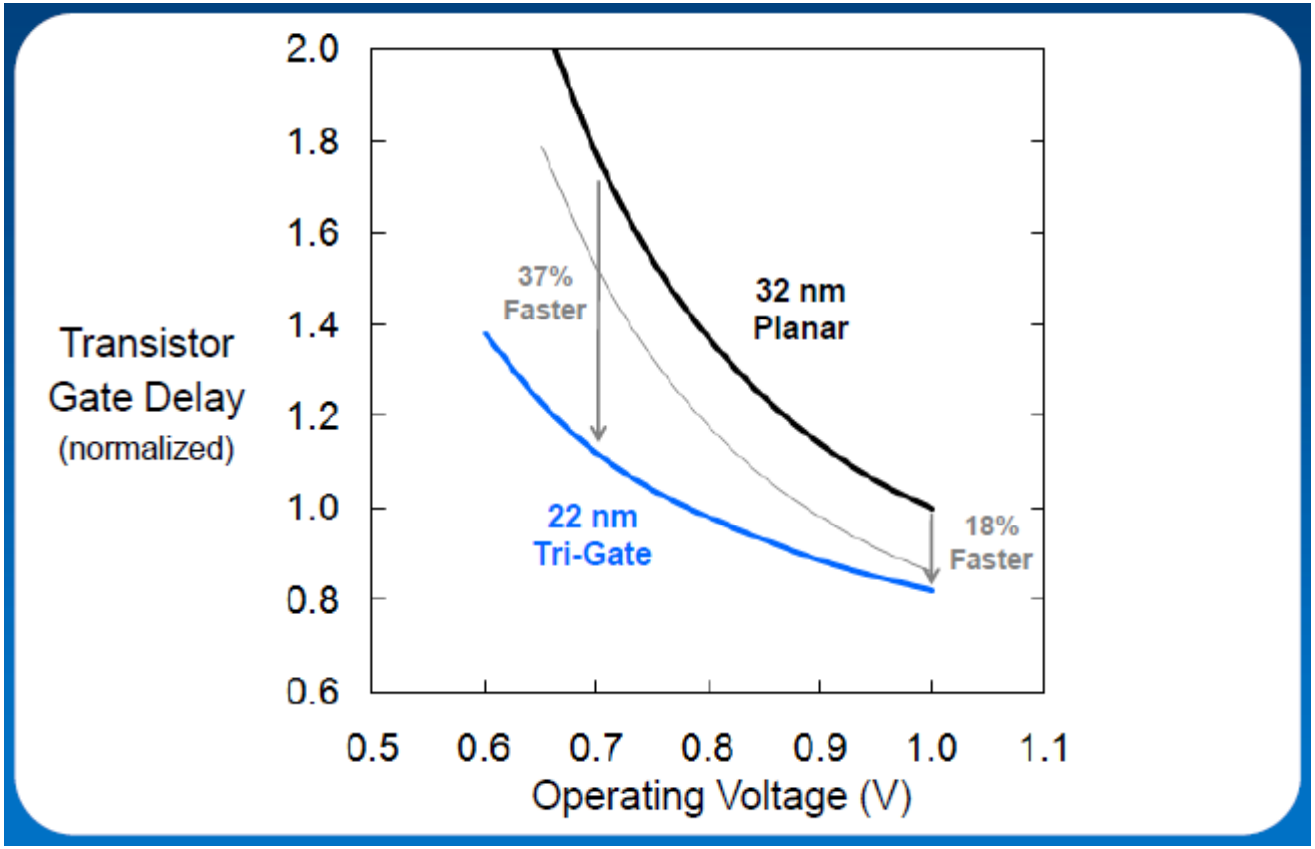
GATE DELAY



Source: Intel May'11

Planar improves over previous node

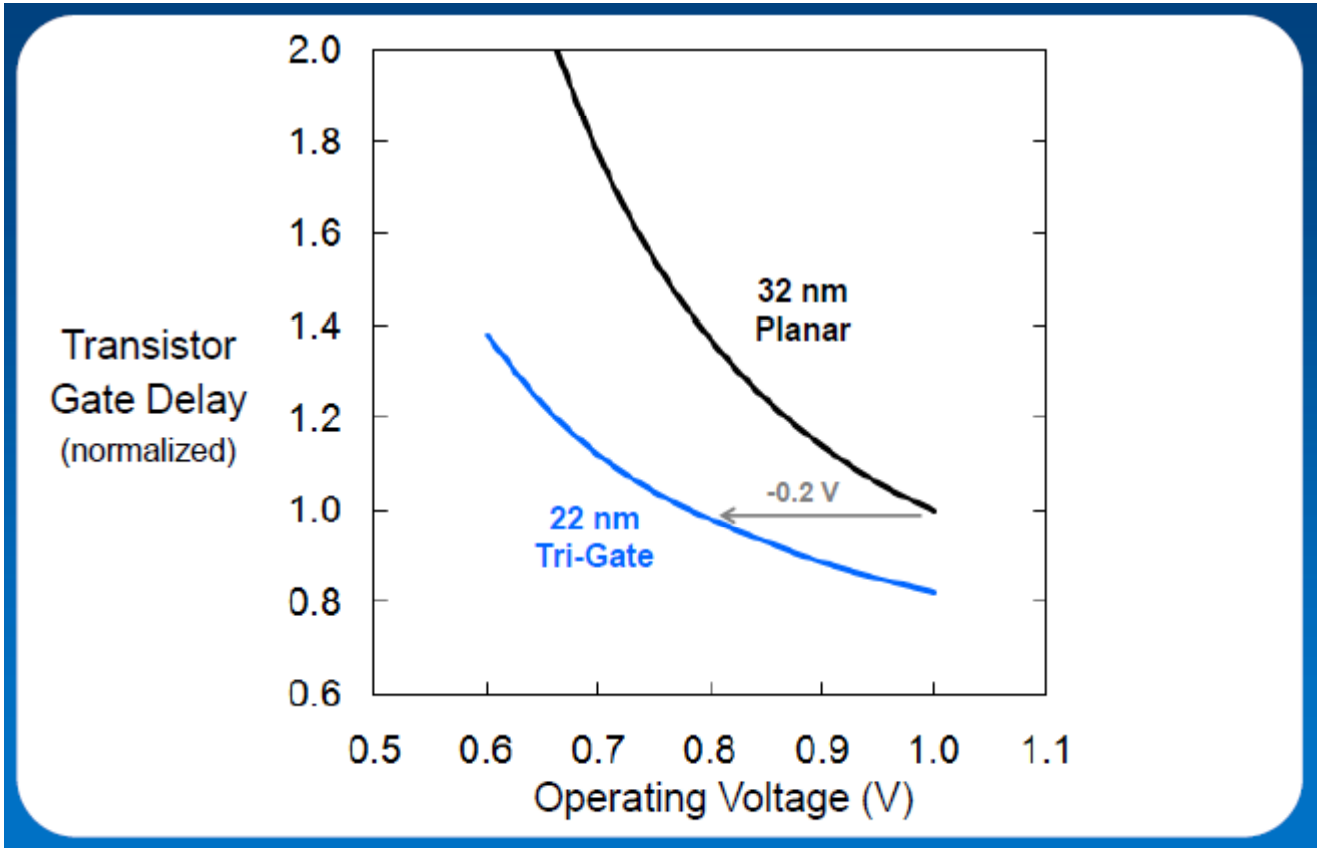
GATE DELAY



Source: Intel May'11

FinFET improves over planar, particular at low Vdd

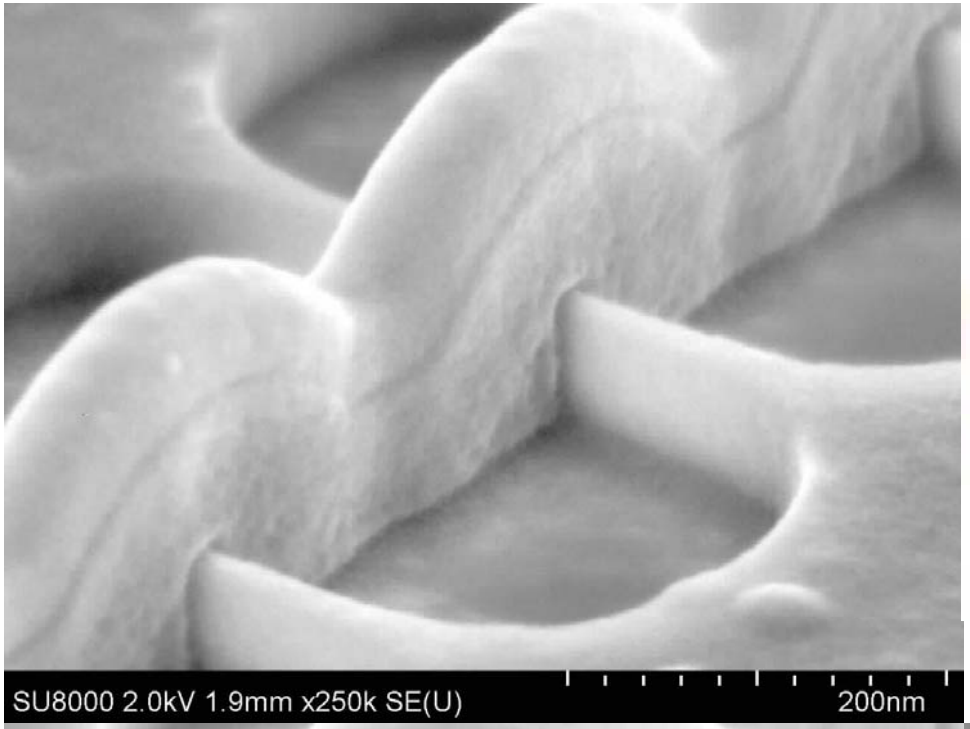
GATE DELAY

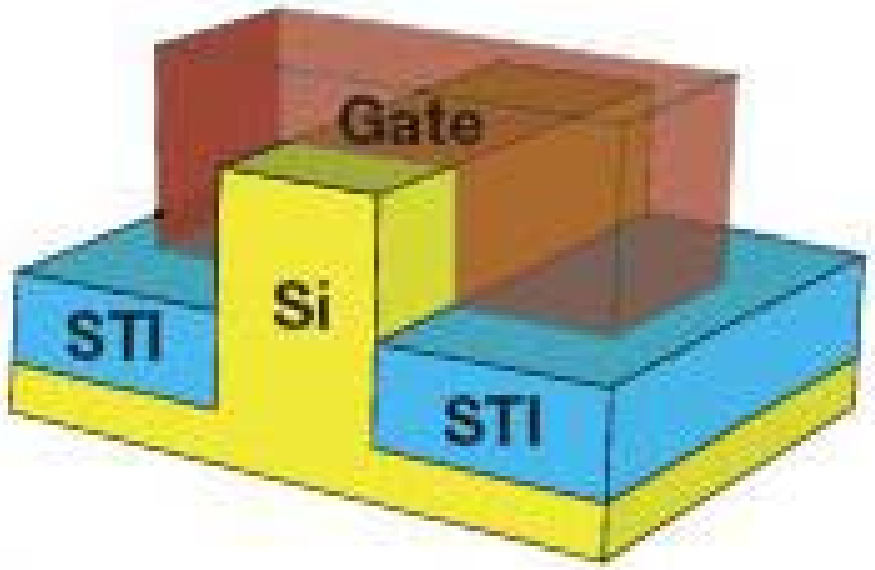


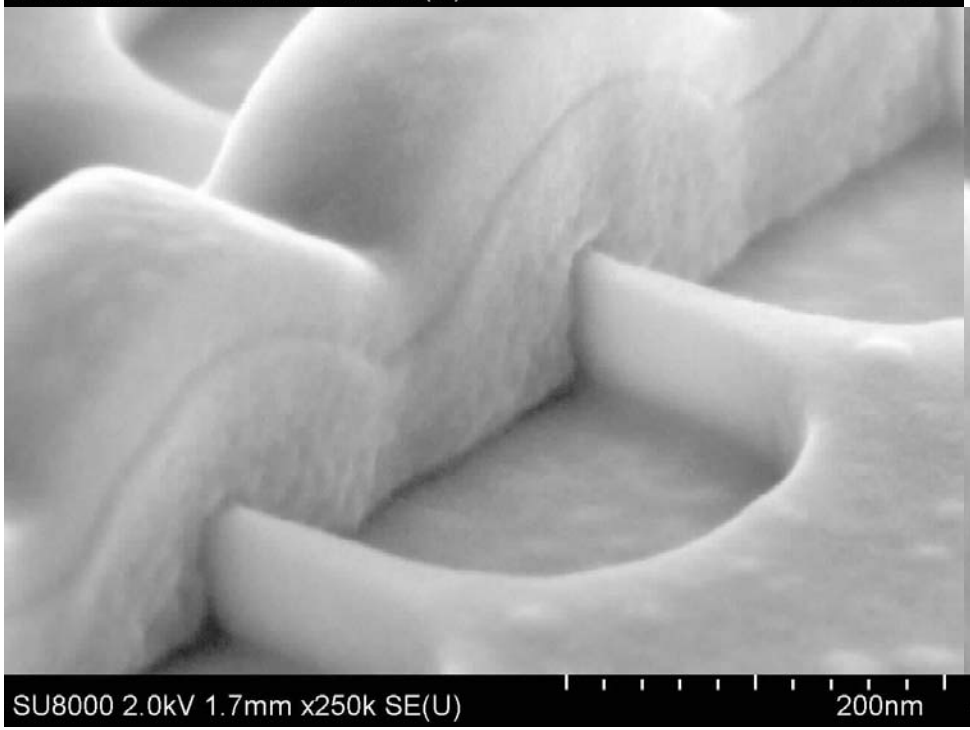
Source: Intel May'11

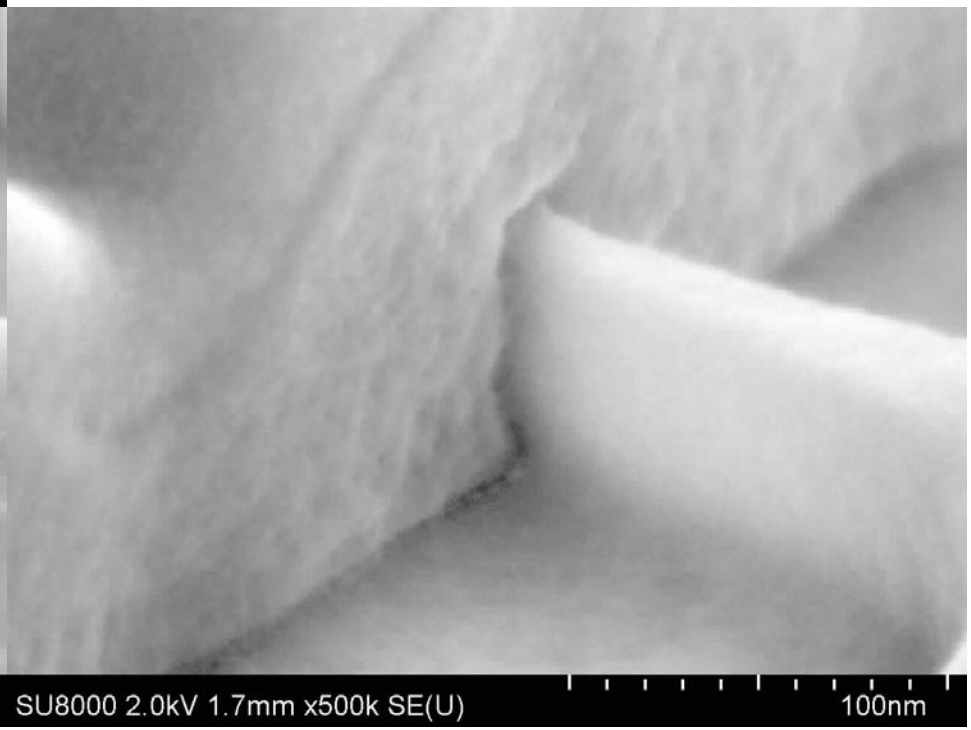
FinFET can operate at lower Vdd, **reducing active power >50%**

Challenges...

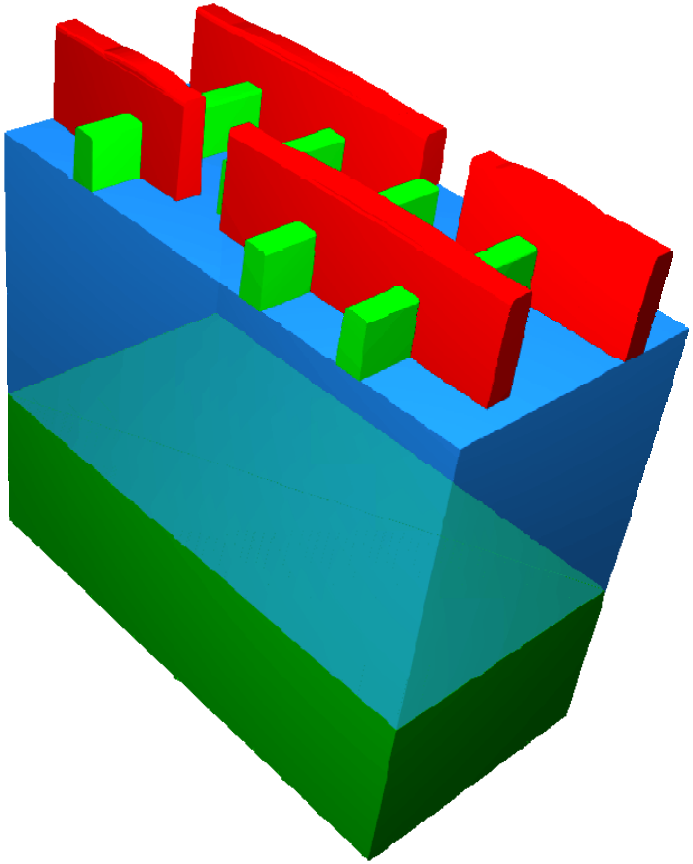

SU8000 2.0kV 1.9mm x250k SE(U)
200nm


Gate
Si
STI
STI

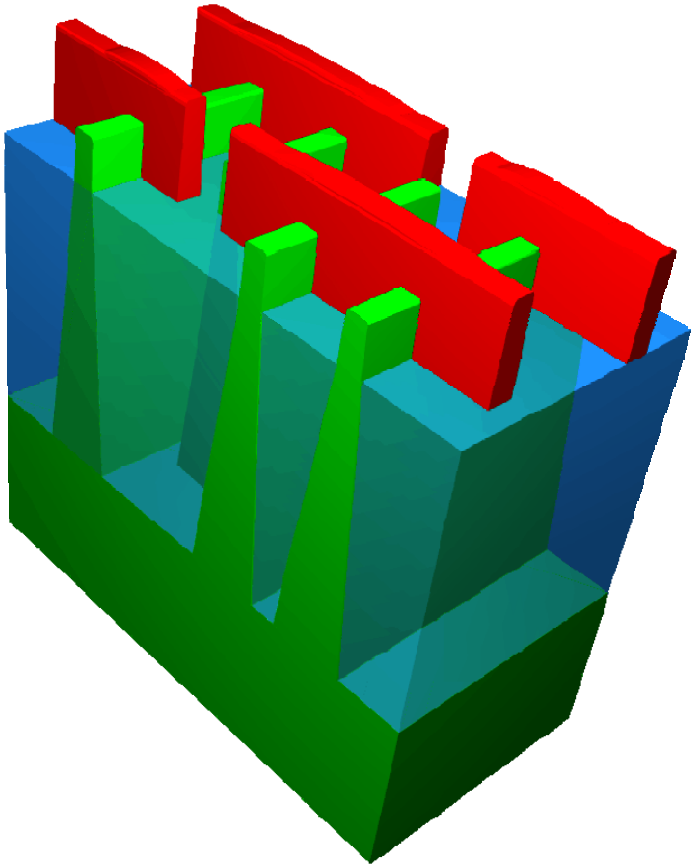

SU8000 2.0kV 1.7mm x250k SE(U)
200nm


SU8000 2.0kV 1.7mm x500k SE(U)
100nm

SOI FF



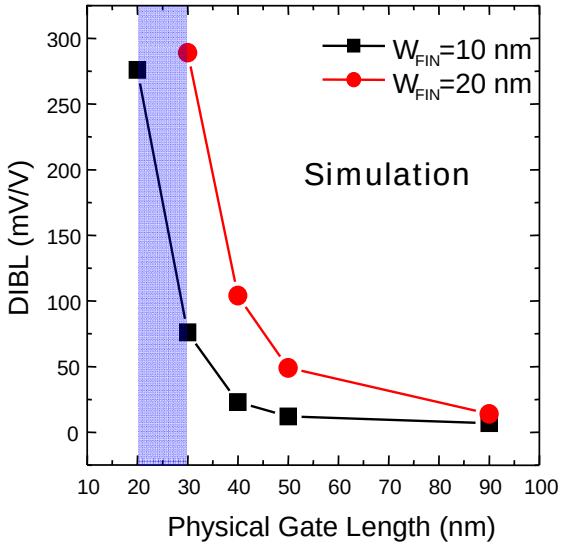
BULK FF

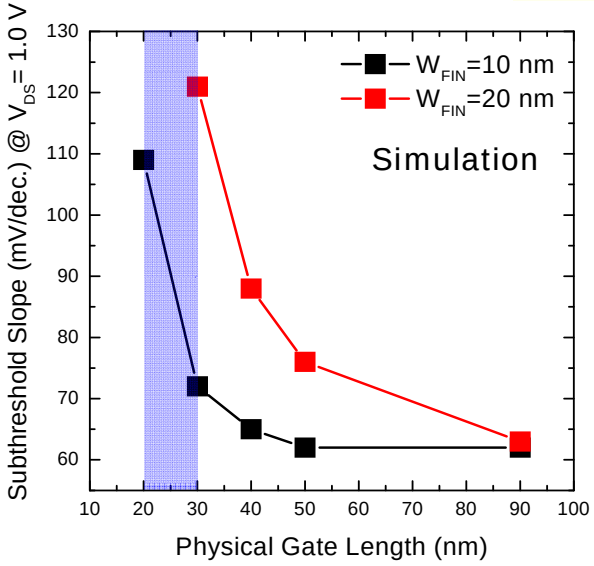


ROADMAP

- LG, W_{FIN}

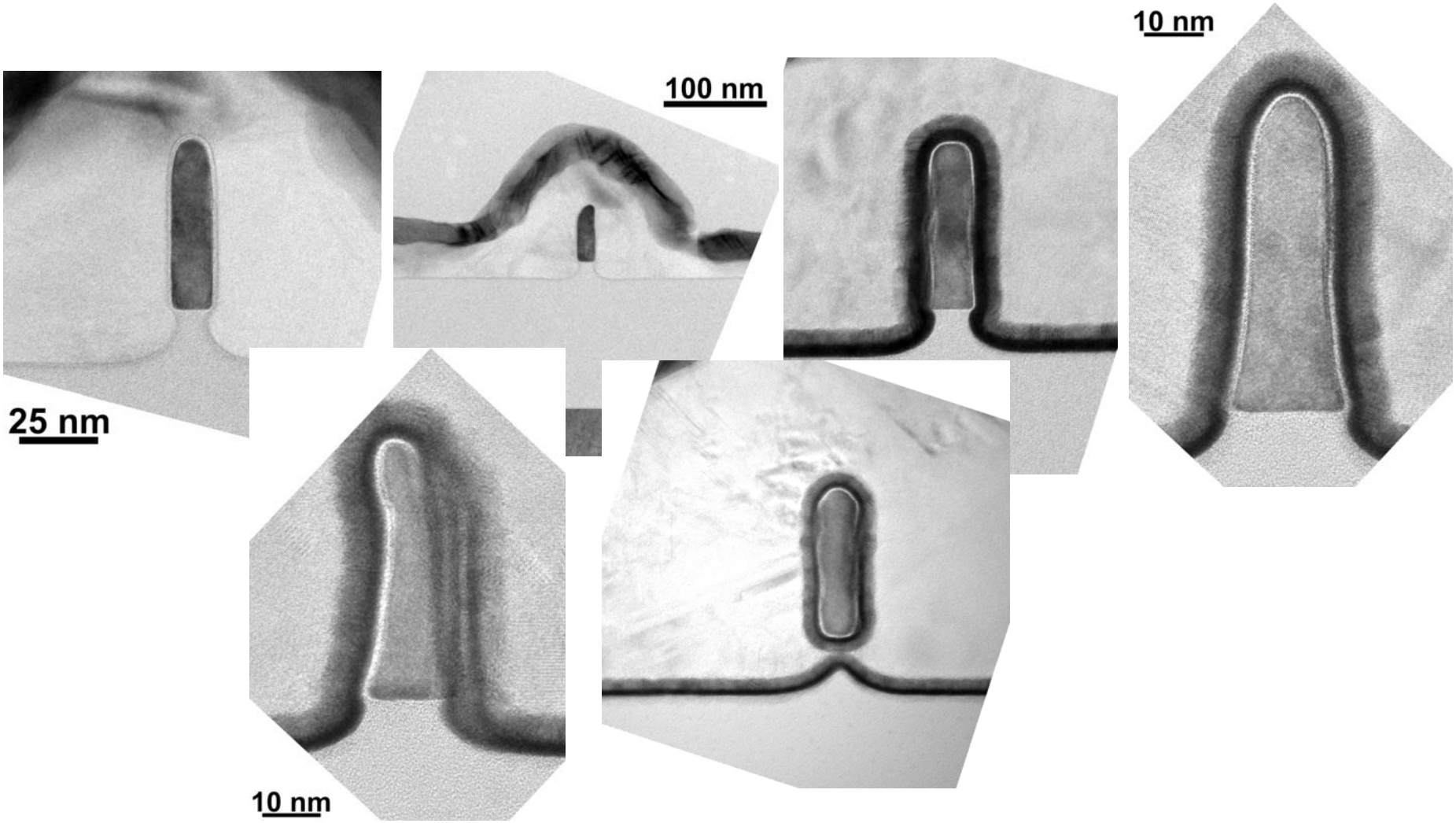
Node	130	90	65	45	32	
Lg	70	56	45	36	32	-20%
W	160	120	80	60	40	0.7x
W_{fin}	-	-	-	23	18	<1/2 Lg





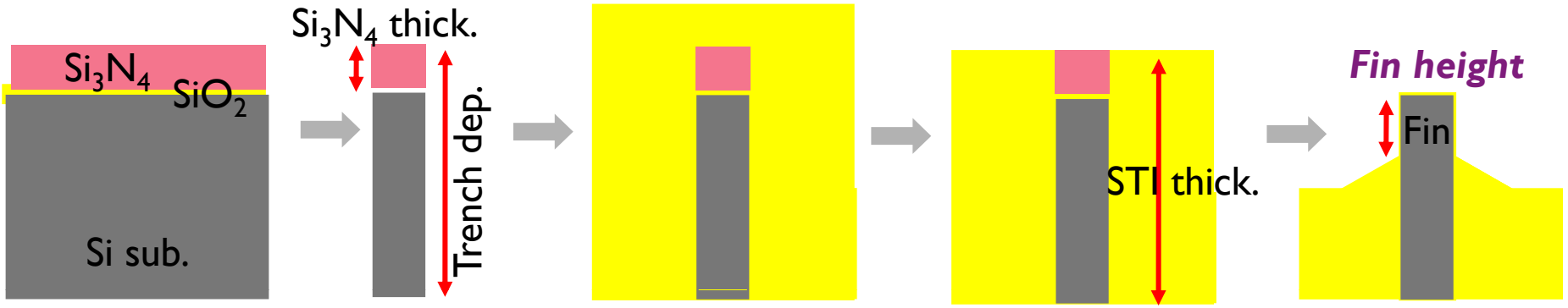
Wfin_target
10-15nm

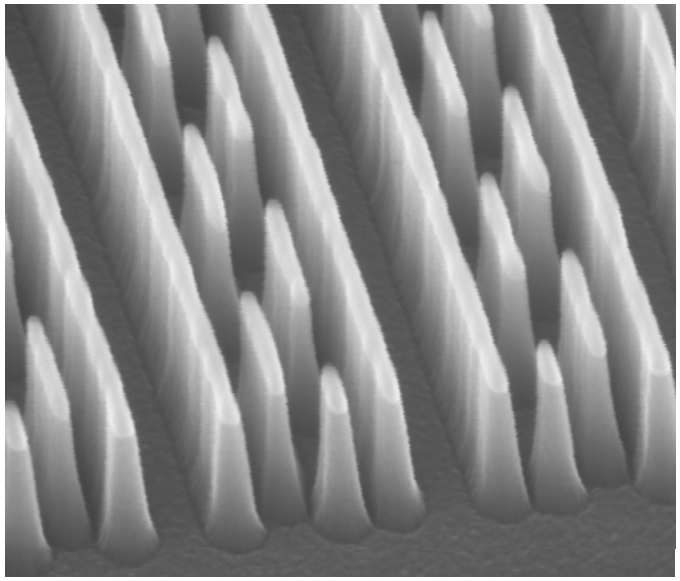
FIN PATTERNING

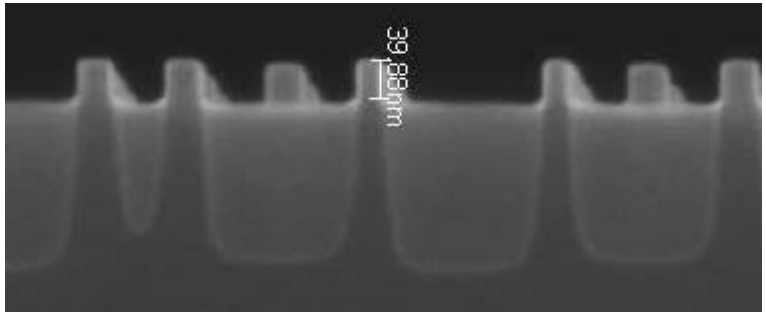


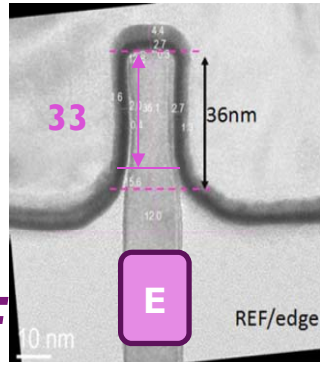
Scaling fins far below lithographic wavelength

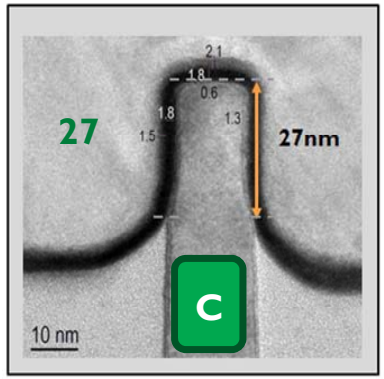
FIN HEIGHT CONTROL





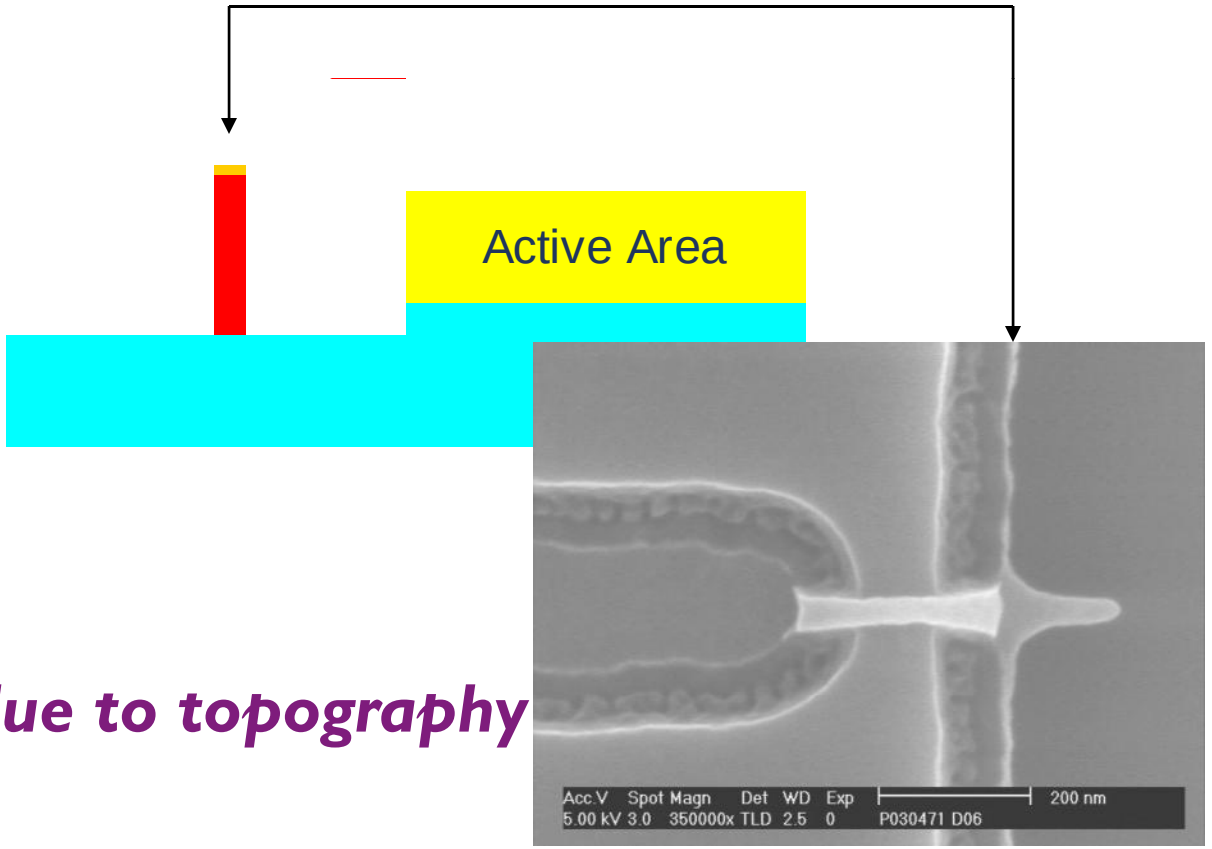






Fin-height control concerns in bulk-FF

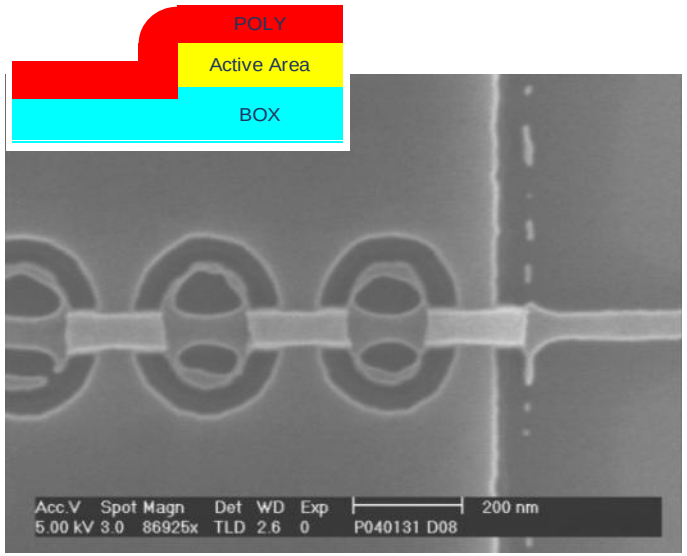
GATE PATTERNING

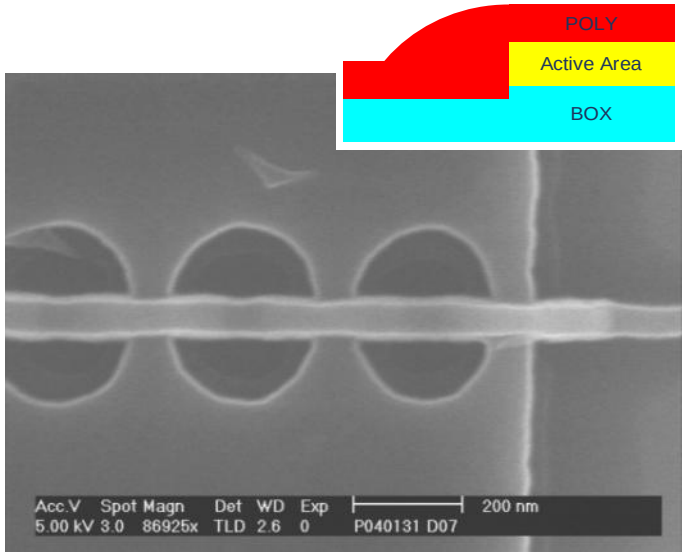


Micro-masking due to topography

GATE PATTERNING

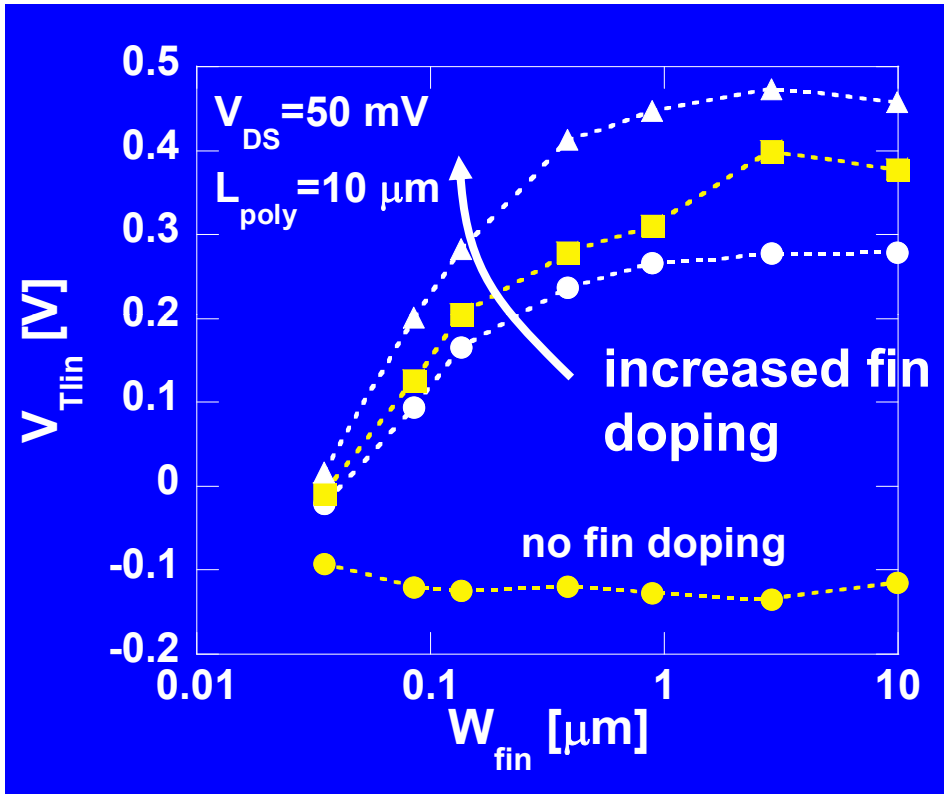
…ETCH-BACK APPROACH…





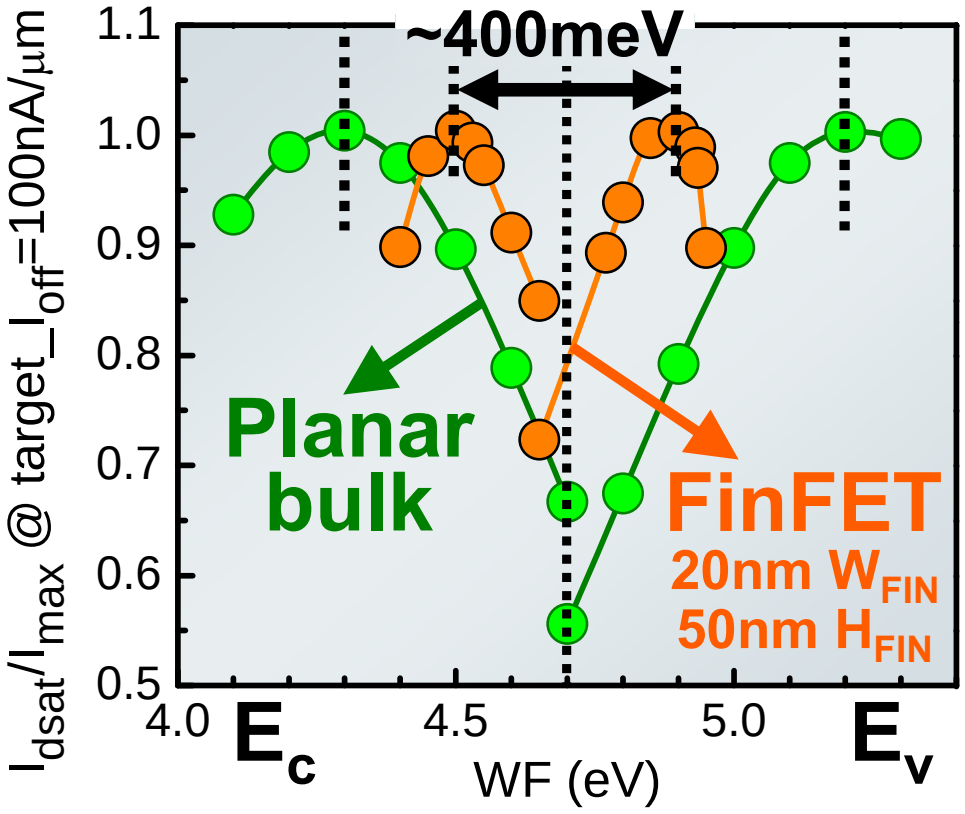
Smoothening the poly transition over fin opens process window

MULTI-VT



At narrow fins, channel doping has no effect on Vt
Need for WF engineering (HKMG)

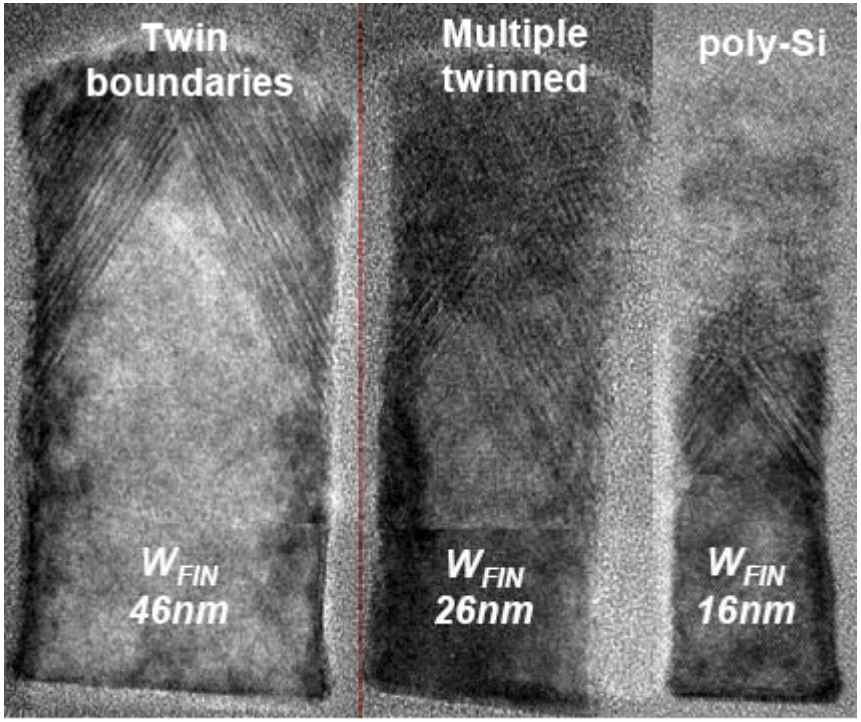
WF-tuning in FinFETs for CMOS



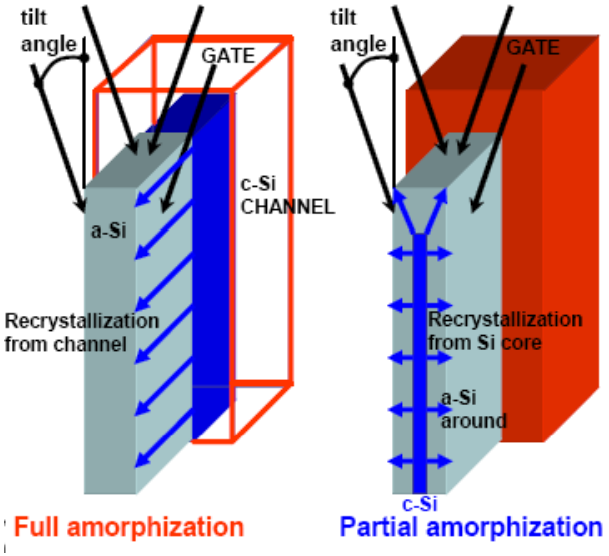
Dual-WF solution needed!

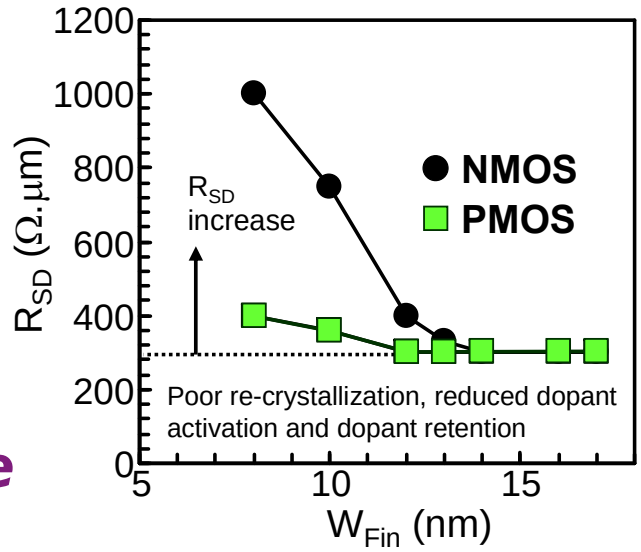
JUNCTION FORMATION

FIN implanted with As + annealed



Duffy, APL, 90, 2007

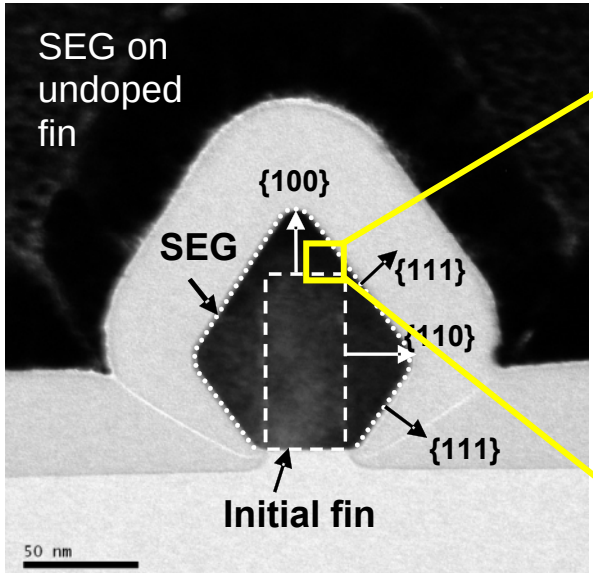


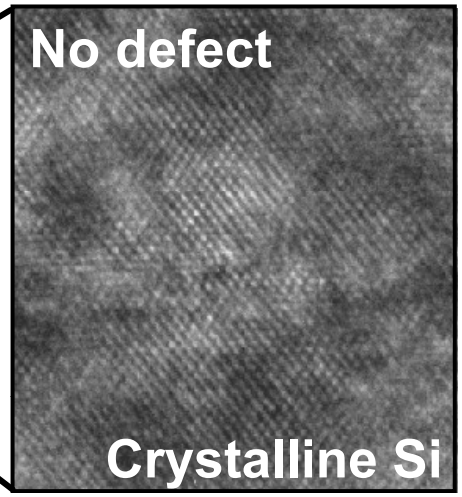


Narrow fins are difficult to recrystallize

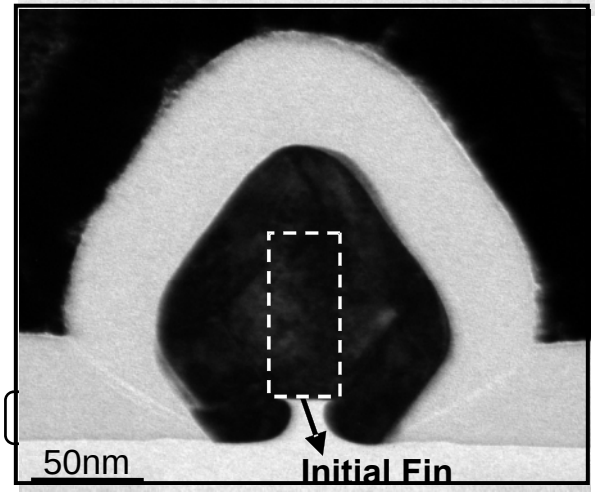
S/D SELECTIVE EPITAXY

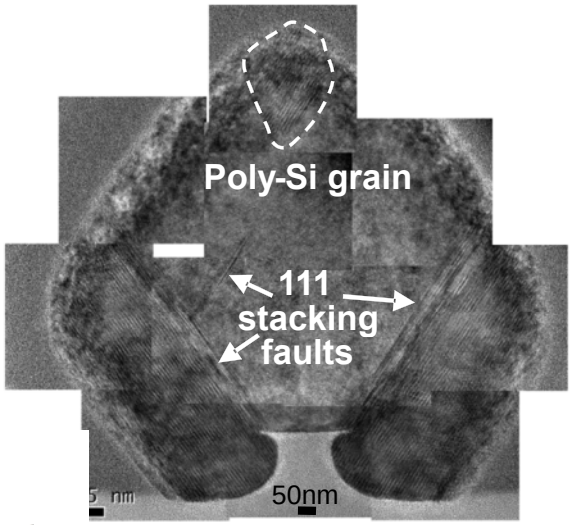
SEG on undoped Fin





SEG on As doped Fin

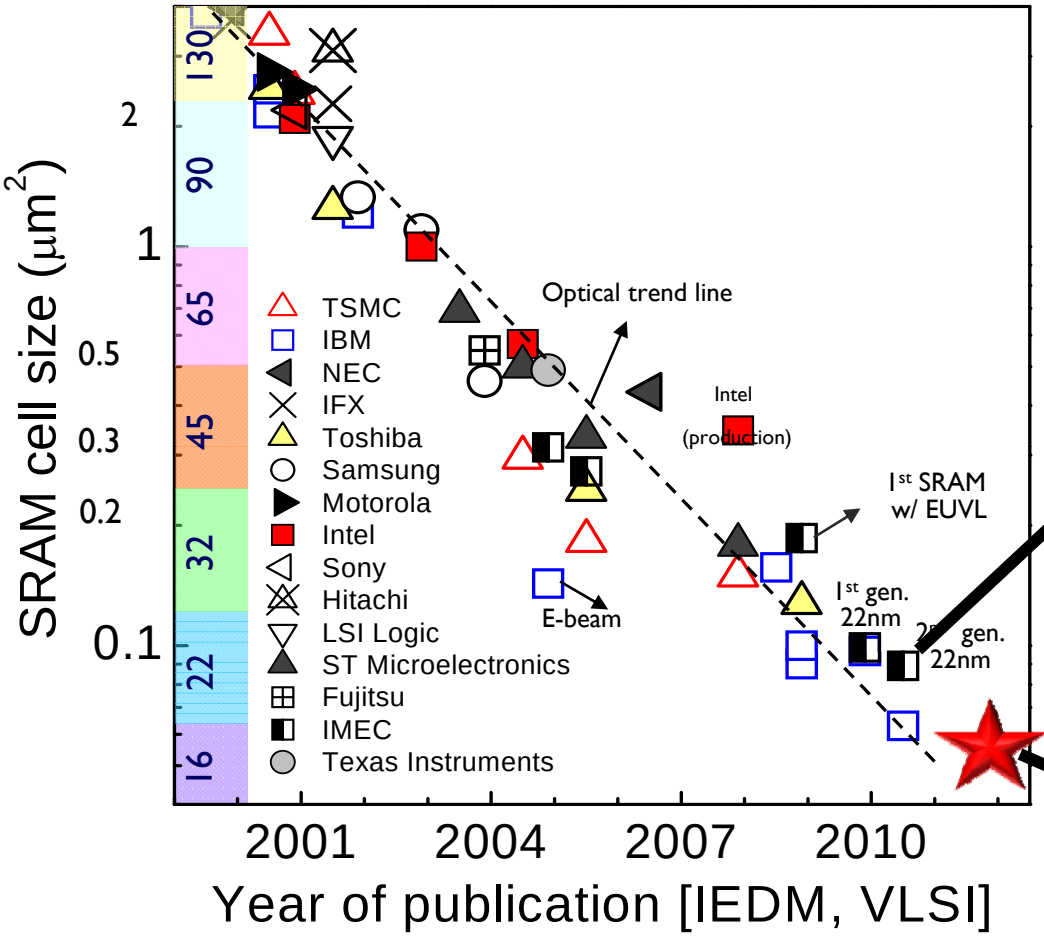


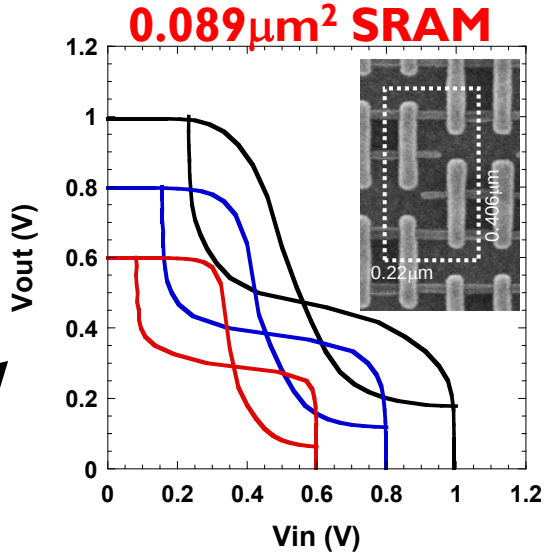


SEG growth & quality depend on S/D implantation

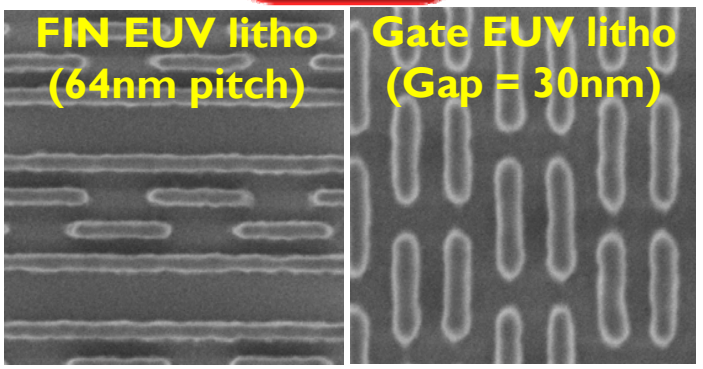
SRAM bit cell

FINFET SCALABILITY SRAM CELL DEMONSTRATORS



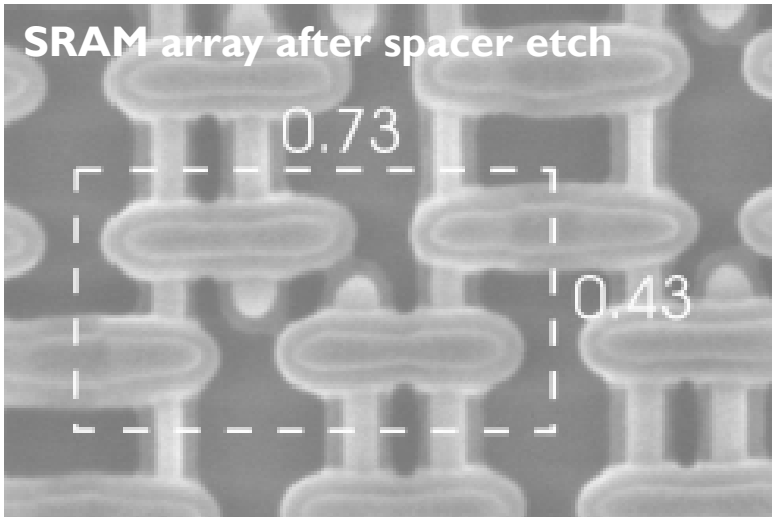


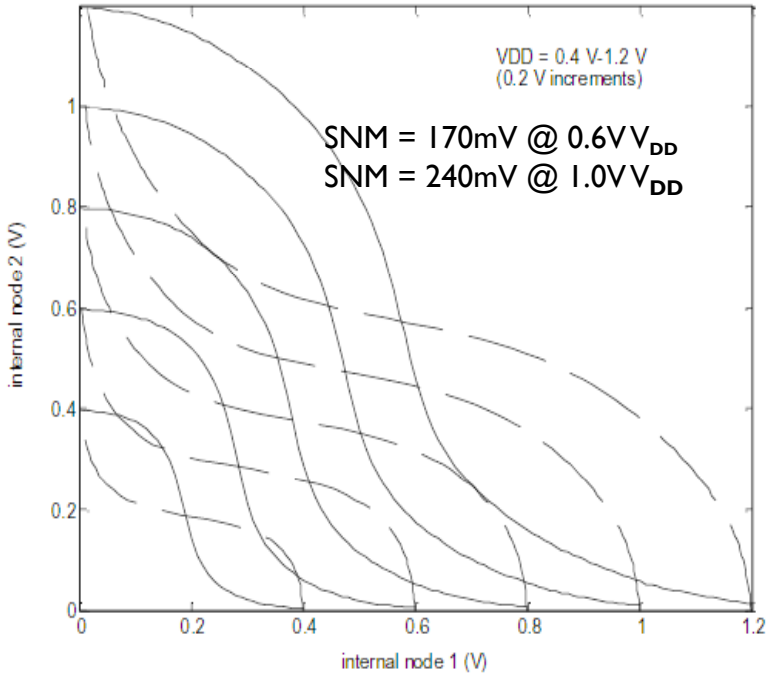
16nm

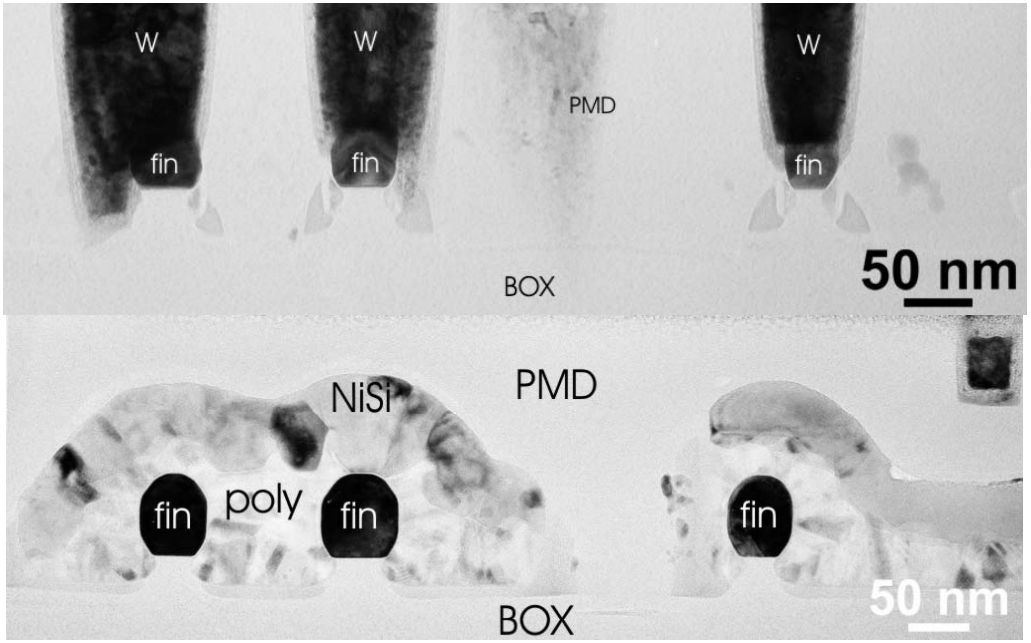


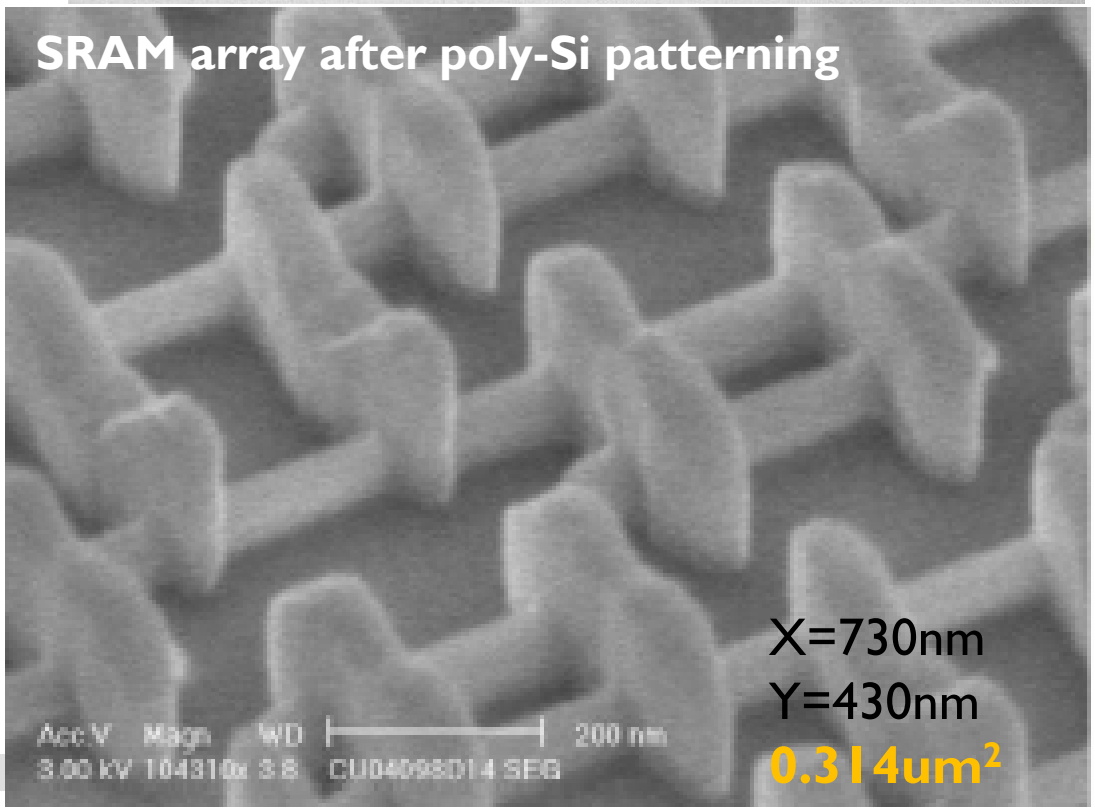
45NM SRAM

(22/06/2004)







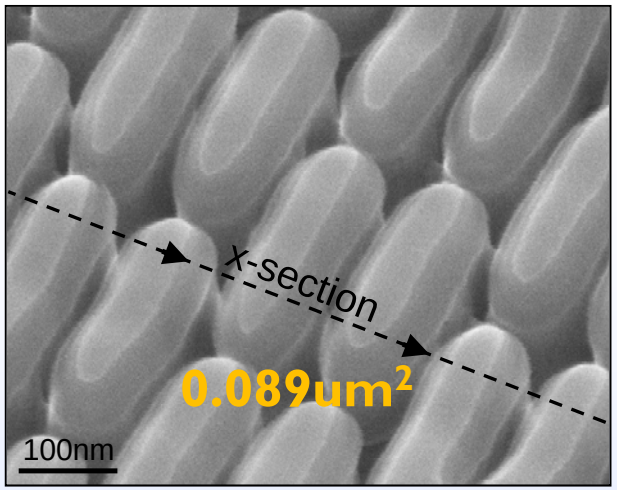


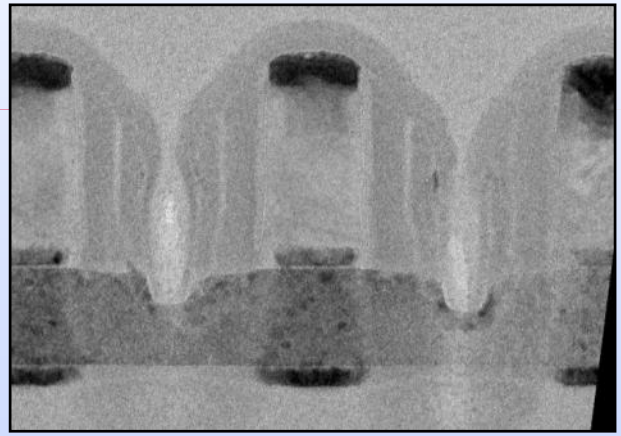
FINFET ENABLES SCALING…

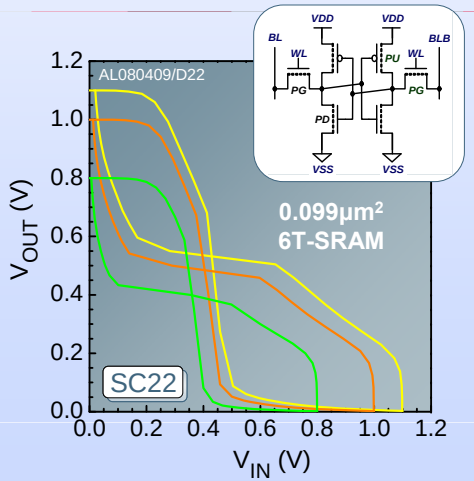
IMEC shows record 22nm SRAM cell density using EUV

(04/22/2009)

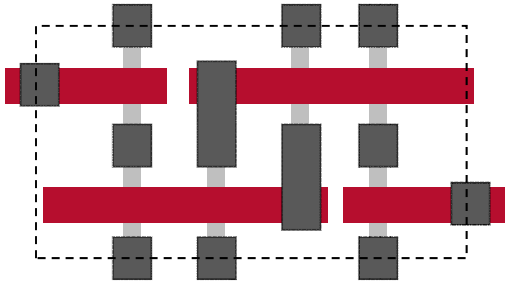
Fully functional 22nm CMOS SRAM cells of 0.089µm² density have been fabricated at IMEC using ASML's EUV Alpha Demo Tool. The R&D facility used its high-k/metal-gate FinFET platform for front-end processing […].

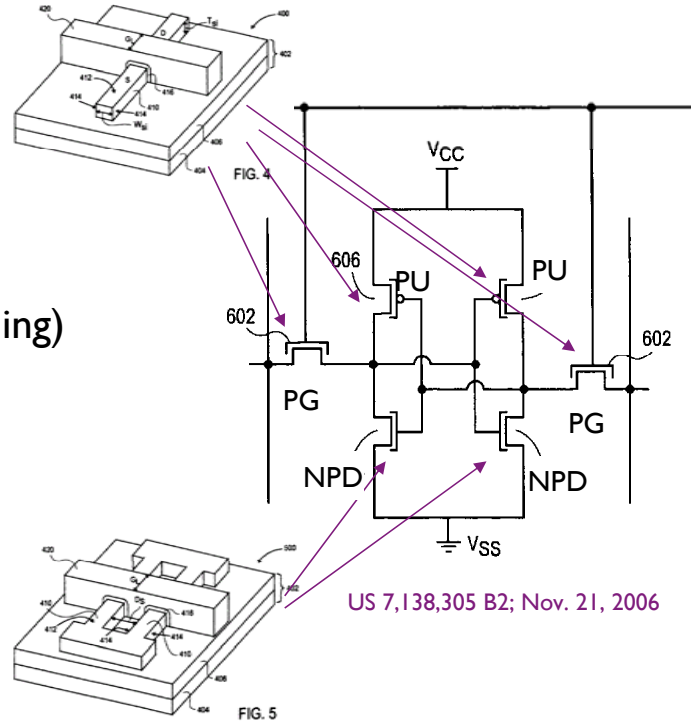




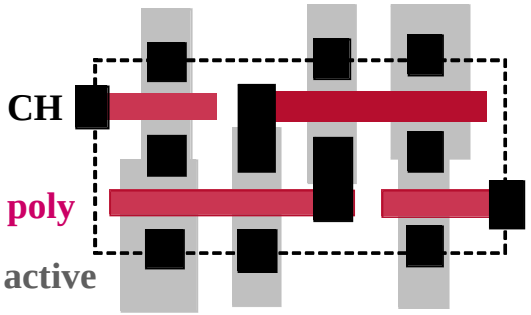


SRAM LAYOUT: PLANAR TO FINFET

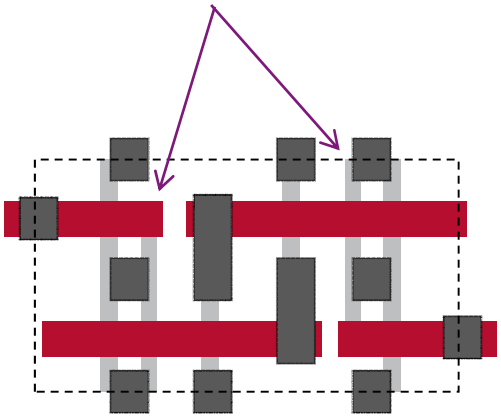




US 7,138,305 B2; Nov. 21, 2006



DPT (Double Patterning)



Summary

SUMMARY

FinFET finally announced for 22nm production ('11)

- After 11 years R&D
- Enables low Vdd operation and chip power savings
- SRAM cells continue to scale with good SNM

Expected to be adopted as mainstream at 16-14nm

Challenges are in process control

- Wfin, Hfin
- Gate profile
- Junction, Strain...

Outlook 11-10nm and beyond ?

- FinFET using non-Si channels...SiGe, IIIV

Thank you !

imec